Data Sheet

μPD720201/μPD720202

ASSP (USB3.0 HOST CONTROLLER)

R19DS0047EJ0600
Rev.6.00
Jan. 29, 2014

1. OVERVIEW

The μPD720201 and μPD720202 are Renesas' third generation Universal Serial Bus 3.0 host controllers, which comply with Universal Serial Bus 3.0 Specification, and Intel's eXtensible Host Controller Interface (xHCI). These devices reduce power consumption and offer a smaller package foot-print making them ideal for designers who wish to add the USB3.0 interface to mobile computing devices such as laptops and notebook computers.

The μPD720201 supports up to four USB3.0 SuperSpeed ports and the μPD720202 supports up to two USB3.0 SuperSpeed ports. The μPD720201 and μPD720202 use a PCI Express® Gen 2 system interface bus allowing system designers to easily add up to four (μPD720201) or two (μPD720202) USB3.0 SuperSpeed ports to systems containing the PCI Express bus interface. When connected to USB 3.0-compliant peripherals, the μPD720201 and μPD720202 can transfer information at clock speeds of up to 5 Gbps. The μPD720201 and μPD720202 and USB3.0 standard are fully compliant and backward compatible with the previous USB2.0 standard. The new USB3.0 standard supports data transfer speeds of up to ten times faster than those of the previous-generation USB2.0 standard, enabling quick and efficient transfers of large amounts of information.

1.1 Features

- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0, which is released by USB Implementers Forum, Inc
    - Supports the following speed data rate as follows: Low-Speed (1.5 Mbps) / Full-Speed (12 Mbps) / Hi-Speed (480 Mbps) / SuperSpeed (5 Gbps)
    - μPD720201 supports up to 4 downstream ports for all speeds
    - μPD720202 supports up to 2 downstream ports for all speeds
    - Supports all USB compliant data transfer types as follows; Control / Bulk / Interrupt / Isochronous transfer
- Compliant with Intel's eXtensible Host Controller Interface (xHCI) Specification Revision 1.0
    - Supports USB debugging capability on all SuperSpeed ports.
- Supports USB legacy function
- Compliant with PCI Express Base Specification Revision 2.0
- Supports Latency Tolerance Reporting ECN of PCI Express Specification
- Supports ExpressCard™ Standard Release1.0
- Supports PCI Express Card Electromechanical Specification Revision 2.0
- Supports PCI Bus Power Management Interface Specification Revision 1.2
- Supports USB Battery Charging Specification Revision 1.2 and other portable devices
    - DCP mode of BC 1.2
    - CDP mode of BC 1.2
    - China Mobile Phone Chargers
    - EU Mobile Phone Chargers
    - Apple iOS products
- Operational registers are direct-mapped to PCI memory space
- Supports Serial Peripheral Interface (SPI) type ROM for Firmware
- Supports Firmware Download Interface from system BIOS or system software
- System clock: 24 MHz crystal

- Small and low count pin package with improved signal pin assignment for efficient PCB layout
  - μPD720201 adopts 68pin QFN (8 x 8)
  - μPD720202 adopts 48pin QFN (7 x 7)
- 3.3 V and 1.05 V power supply

1.2 Applications

Desktop and Laptop computers, Tablet, Server, PCI Express Card / Express Card, Digital TV, Set-Top-Box, BD Player/Recorder, Media Player, Digital Audio systems, Projector, Multi Function Printer, Storage, Router, NAS, etc

1.3 Ordering Information

Part Number	Package	Operating temperature	Remark
μPD720201K8-701-BAC-A	68-pin QFN (8 × 8)	0 to 85 °C	Lead-free product
μPD720202K8-701-BAA-A	48-pin QFN (7 x 7)		Lead-free product
μPD720201K8-711-BAC-A	68-pin QFN (8 × 8)	–40 to 85 °C	Lead-free product
μPD720202K8-711-BAA-A	48-pin QFN (7 x 7)		Lead-free product

Note μPD720201K8-711-BAC-A & μPD720202K8-711-BAA-A should use the FW Download function.
μPD720201K8-711-BAC-A & μPD720202K8-711-BAA-A do not support the External ROM (Serial Peripheral Interface (SPI) type ROM).
μPD720201 & μPD720202 should download the firmware from the External ROM (-701 versions only) or by FW download function after Power on Reset.
Regarding the External ROM & FW Download function, refer to “6.How to Access External ROM” & “7. FW Download Interface” in the μPD720201 & μPD720202 User’s manual : R19UH0078E.

1.4 Block Diagram

Figure 1-1. μPD720201 Block Diagram

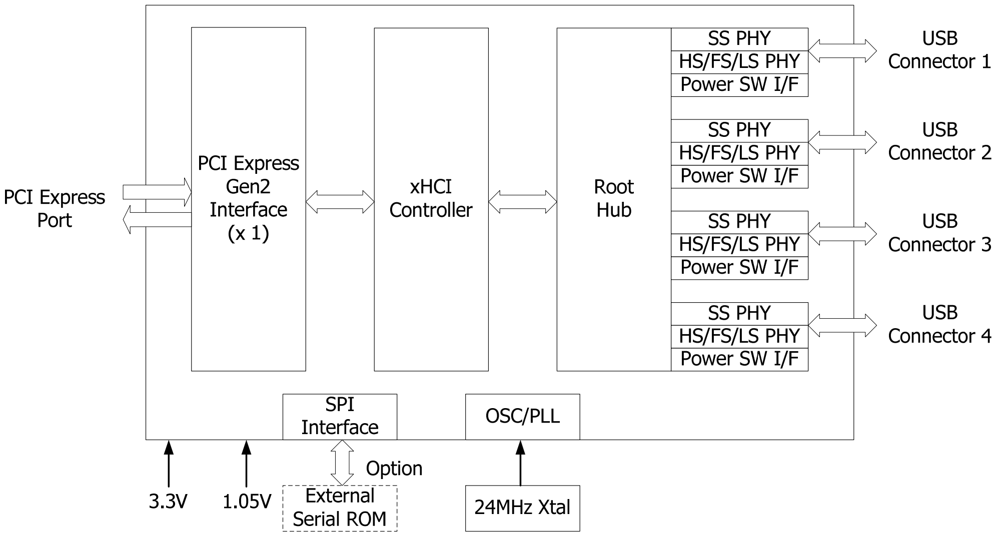
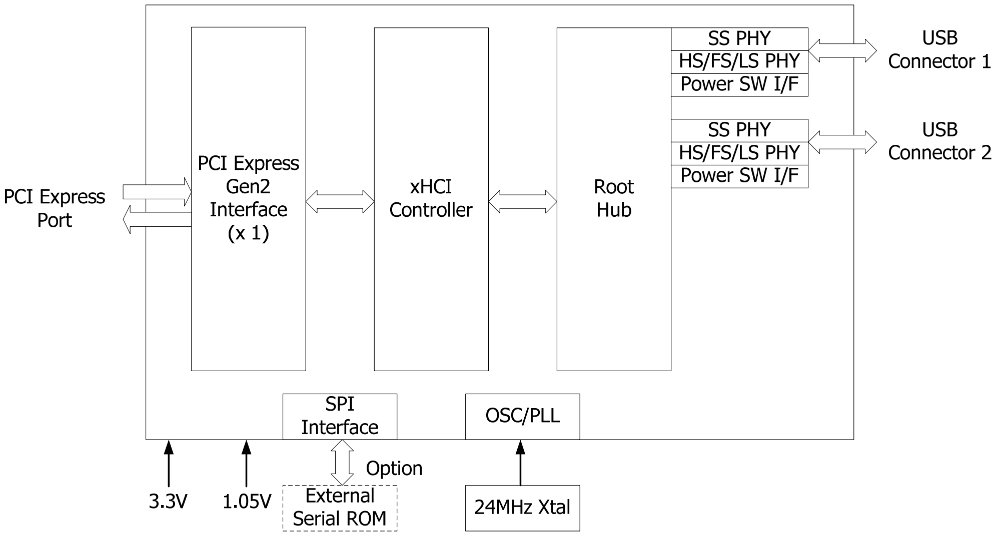


Figure 1-2. μPD720202 Block Diagram



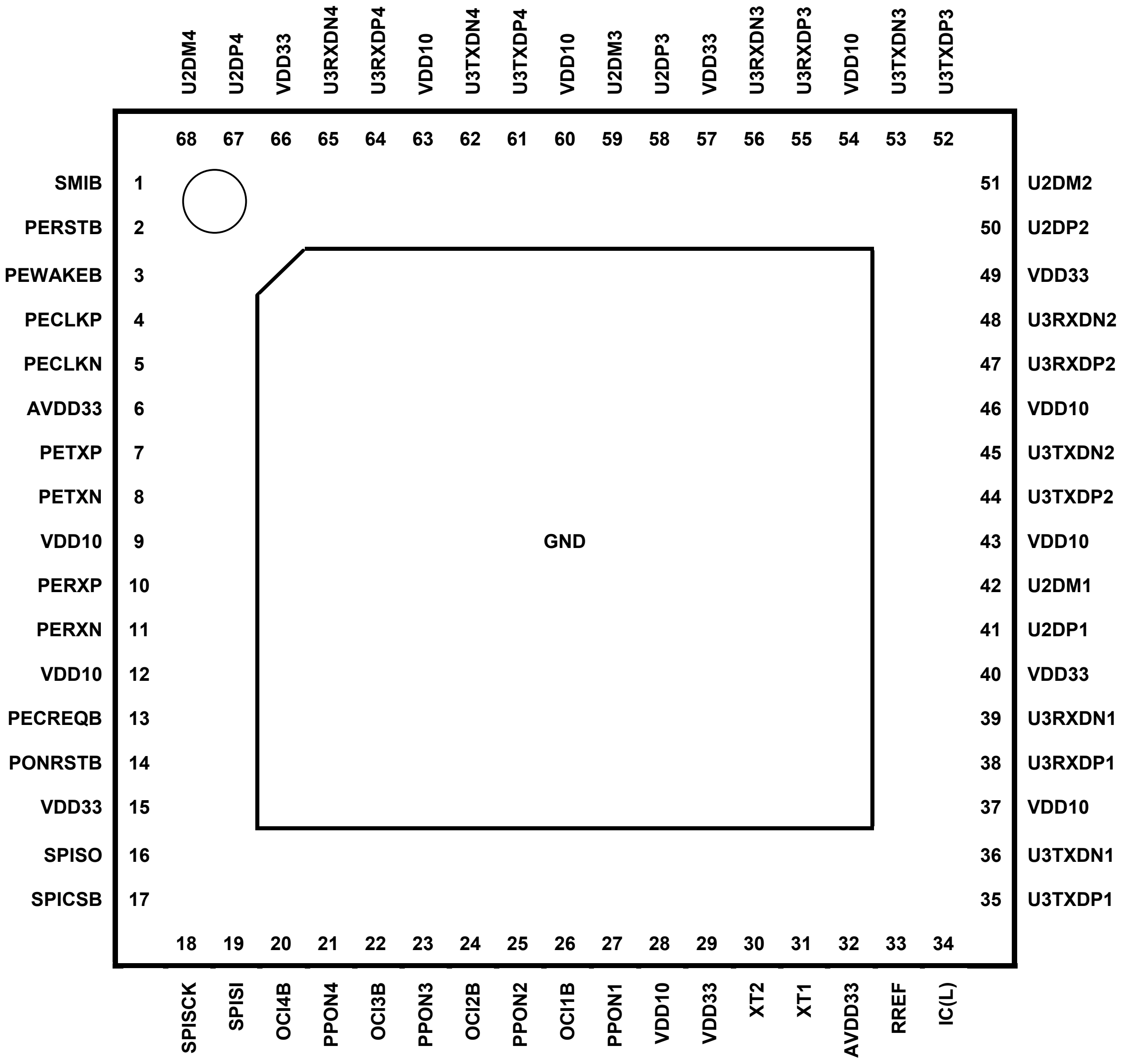
PCI Express Gen2 Interface	Complies with PCI Express Gen2 interface, with 1 lane. This block includes both the link and PHY layers.
xHCI Controller	Handles all support required for USB 3.0, SuperSpeed and Hi-/Full-/Low-speed. This block includes the register interface from the system.
Root hub	Hub function in host controller.
SS PHY	For SuperSpeed Tx/Rx
HS/FS/LS PHY	For Hi-/Full-/Low-Speed Tx/Rx
Power SW I/F	Connected to external power switch for port power control and over current detection.
SPI Interface	Connected to external serial ROM. When system BIOS or system software does not support FW download function, the external serial ROM is required.
OSC	Internal oscillator block.

1.5 Pin Configuration (TOP VIEW)

- **68-pin QFN (8 × 8)**
  μPD720201K8-701-BAC-A

  μPD720201K8-711-BAC-A

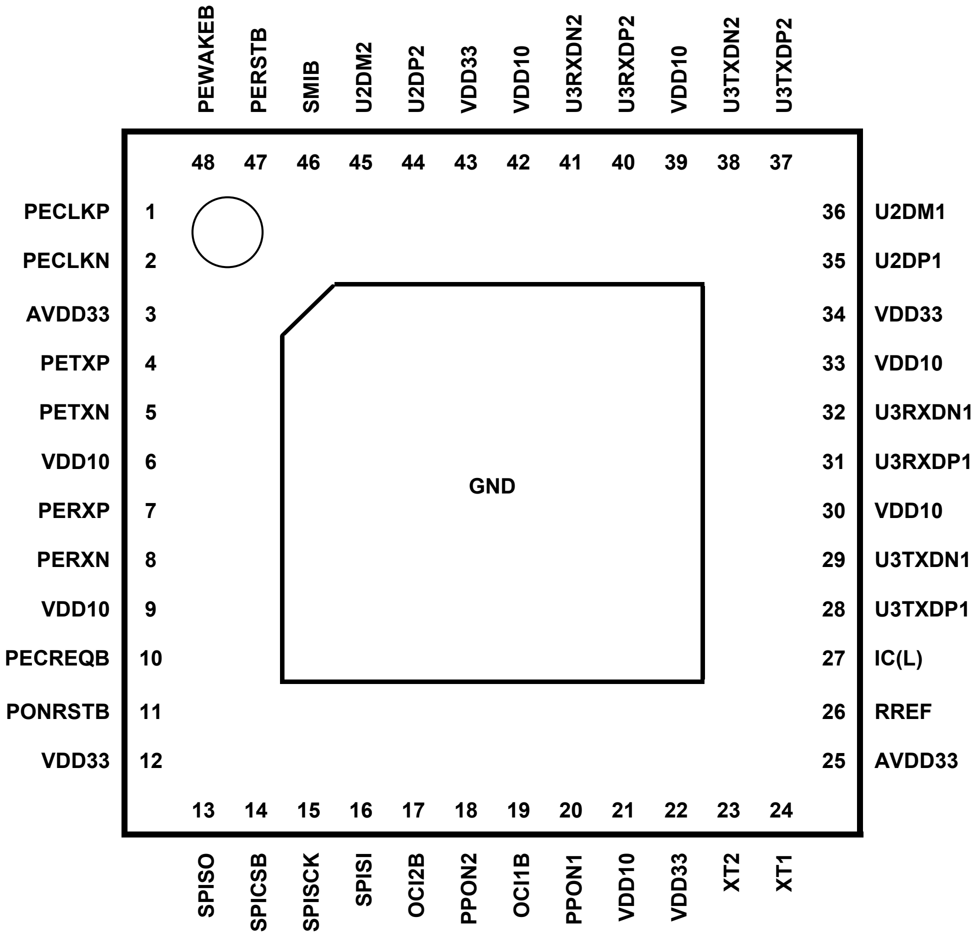
Figure 1-3. Pin Configuration of μPD720201



- **48-pin QFN (7 x 7)**
  μPD720202K8-701-BAA-A

  μPD720202K8-711-BAA-A

Figure 1-4. Pin Configuration of μPD720202



2. PIN FUNCTION

This section describes each pin functions.

2.1 Power supply

Table 2-1. Power Supply

Pin Name	μPD720201 Pin No.	μPD720202 Pin No.	I/O Type	Function
VDD33	15, 29, 40, 49, 57, 66	12, 22, 34, 43	Power	+3.3 V power supply
VDD10	9, 12, 28, 37, 43, 46, 54, 60, 63	6, 9, 21, 30, 33, 39, 42	Power	+1.05 V power supply.
AVDD33	6, 32	3, 25	Power	+3.3 V power supply for analog circuit.
GND	GND PAD	GND PAD	Power	Connect to ground.
IC(L)	34	27	I	Test pin. Connect to ground.

2.2 Analog Signal

Table 2-2. Analog Signal

Pin Name	720201 Pin No.	720202 Pin No.	I/O Type	Active Level	Function
RREF	33	26	USB2	–	Reference resistor connection.

2.3 System clock

Table 2-3. System Clock

Pin Name	720201 Pin No.	720202 Pin No.	Type	Active Level	Function
XT1	31	24	I (OSC)	–	Oscillator in Connect to 24 MHz crystal.
XT2	30	23	O (OSC)	–	Oscillator out Connect to 24 MHz crystal.

2.3.1 System Interface signal

Table 2-4. System Interface Signal

Pin Name	720201 Pin No.	720202 Pin No.	I/O Type	Active Level	Function
PONRSTB	14	11	I (3.3 V Schmitt Input)	Low	Power on reset signal. When supporting wakeup from D3cold, this signal should be pulled high with system auxiliary power supply.
SMIB	1	46	O (Open Drain)	Low	System management Interrupt signal. This is controlled with the USB Legacy Support Control/Status register. Refer to the User's Manual.

2.3.2 PCI Express Interface

Table 2-5. PCI Express Interface

Pin Name	720201 Pin No.	720202 Pin No.	I/O Type	Active Level	Function
PECLKP	4	1	I (PCIE)	–	PCI Express 100 MHz Reference Clock.
PECLKN	5	2	I (PCIE)	–	PCI Express 100 MHz Reference Clock.
PETXP	7	4	O (PCIE)	–	PCI Express Transmit Data+.
PETXN	8	5	O (PCIE)	–	PCI Express Transmit Data-.
PERXP	10	7	I (PCIE)	–	PCI Express Receive Data+.
PERXN	11	8	I (PCIE)	–	PCI Express Receive Data-.
PERSTB	2	47	I (3.3 V Input)	Low	PCI Express "PERST#" signal.
PEWAKEB	3	48	O (Open Drain)	Low	PCI Express "WAKE#" signal. This signal is used for remote wakeup mechanism, and requests the recovery of power and reference clock input.
PECREQB	13	10	O (Open Drain)	Low	PCI Express "CLKREQ#" signal. This signal is used to request run/stop of reference clock.

2.3.3 USB Interface

Table 2-6. USB Interface

Pin Name	720201 Pin No.	720202 Pin No.	I/O Type	Active Level	Function
U3TXDP1	35	28	O (USB3)	–	USB3.0 Transmit data D+ signal for SuperSpeed
U3TXDN1	36	29	O (USB3)	–	USB3.0 Transmit data D- signal for SuperSpeed
U3RXDP1	38	31	I (USB3)	–	USB3.0 Receive data D+ signal for SuperSpeed
U3RXDN1	39	32	I (USB3)	–	USB3.0 Receive data D- signal for SuperSpeed
U2DP1	41	35	I/O (USB2)	–	USB2.0 D+ signal for Hi-/Full-/Low-Speed
U2DM1	42	36	I/O (USB2)	–	USB2.0 D– signal for Hi-/Full-/Low-Speed
OCI1B	26	19	I (3.3 V Input)	Low	Over-current status input signal. 0: Over-current condition is detected 1: No over-current condition is detected
PPON1	27	20	O (3.3 V Output)	High	USB port power supply control signal. 0: Power supply OFF 1: Power supply ON
U3TXDP2	44	37	O (USB3)	–	USB3.0 Transmit data D+ signal for SuperSpeed
U3TXDN2	45	38	O (USB3)	–	USB3.0 Transmit data D- signal for SuperSpeed
U3RXDP2	47	40	I (USB3)	–	USB3.0 Receive data D+ signal for SuperSpeed
U3RXDN2	48	41	I (USB3)	–	USB3.0 Receive data D- signal for SuperSpeed
U2DP2	50	44	I/O (USB2)	–	USB2.0 D+ signal for Hi-/Full-/Low-Speed
U2DM2	51	45	I/O (USB2)	–	USB2.0 D– signal for Hi-/Full-/Low-Speed
OCI2B	24	17	I (3.3 V Input)	Low	Over-current status input signal. 0: Over-current condition is detected 1: No over-current condition is detected
PPON2	25	18	O (3.3 V Output)	High	USB port power supply control signal. 0: Power supply OFF 1: Power supply ON

Pin Name	720201 Pin No.	720202 Pin No.	I/O Type	Active Level	Function
U3TXDP3	52	–	O (USB3)	–	USB3.0 Transmit data D+ signal for SuperSpeed
U3TXDN3	53	–	O (USB3)	–	USB3.0 Transmit data D- signal for SuperSpeed
U3RXDP3	55	–	I (USB3)	–	USB3.0 Receive data D+ signal for SuperSpeed
U3RXDN3	56	–	I (USB3)	–	USB3.0 Receive data D- signal for SuperSpeed
U2DP3	58	–	I/O (USB2)	–	USB2.0 D+ signal for Hi-/Full-/Low-Speed
U2DM3	59	–	I/O (USB2)	–	USB2.0 D– signal for Hi-/Full-/Low-Speed
OCI3B	22	–	I (3.3 V Input)	Low	Over-current status input signal. 0: Over-current condition is detected 1: No over-current condition is detected
PPON3	23	–	O (3.3 V Output)	High	USB port power supply control signal. 0: Power supply OFF 1: Power supply ON
U3TXDP4	61	–	O (USB3)	–	USB3.0 Transmit data D+ signal for SuperSpeed
U3TXDN4	62	–	O (USB3)	–	USB3.0 Transmit data D- signal for SuperSpeed
U3RXDP4	64	–	I (USB3)	–	USB3.0 Receive data D+ signal for SuperSpeed
U3RXDN4	65	–	I (USB3)	–	USB3.0 Receive data D- signal for SuperSpeed
U2DP4	67	–	I/O (USB2)	–	USB2.0 D+ signal for Hi-/Full-/Low-Speed
U2DM4	68	–	I/O (USB2)	–	USB2.0 D– signal for Hi-/Full-/Low-Speed
OCI4B	20	–	I (3.3 V Input)	Low	Over-current status input signal. 0: Over-current condition is detected 1: No over-current condition is detected
PPON4	**21**	–	**O (3.3 V Output)**	**High**	**USB port power supply control signal.** **0: Power supply OFF** **1: Power supply ON**

Note 1: The SuperSpeed signals (U3TXDPx, U3TXDNx, U3RXDPx, U3RXDNx) and high-/full-/low-signals (U2DPx, U2DMx) of μPD720201 and μPD720202 shall be connected to the same USB connecter, Refer to μPD720201/μPD720202 User's Manual.

Note 2: The Timing of PPONx assertion is changed from μPD720200. The PPONx of μPD720200A, μPD720201 and μPD720202 are asserted after the software sets Max Device Slots Enable(MaxSlotsEn) field in Configure(CONFIG) register or Host Controller Reset(HCRST) flag in USBCMD register. On μPD720200, the PPON(2:1) are asserted immediately after the PCIe Reset. Regarding the CONFIG and USBCMD register, refer to the μPD720201/μPD720202 User's Manual.

2.3.4 SPI Interface

Table 2-7. SPI Interface

Pin Name	720201 Pin No.	720202 Pin No.	Type	Active Level	Function
SPISCK	18	15	O (3.3 V Output)	–	SPI serial flash ROM clock signal. When the external serial ROM is not mounted, this signal should be pulled down through a pull-down resistor.
SPICSB	17	14	O (3.3 V Output)	–	SPI serial flash ROM chip select signal. When the external serial ROM is not mounted, this signal should be pulled down through a pull-down resistor.
SPISI	19	16	O (3.3 V Output)	–	SPI serial flash ROM slave input signal. When the external serial ROM is not mounted, this signal should be pulled down through a pull-down resistor.
SPISO	16	13	I (3.3 V Input)	-	SPI serial flash ROM slave output signal. This signal should be pulled up through a pull-up resistor in all cases.

3. ELECTRICAL SPECIFICATIONS

3.1 Buffer List

- 3.3 V input buffer

  OCI(4:1)B, PERSTB, IC(L)
- 3.3 V input schmitt buffer

  PONRSTB
- 3.3 V I_{OLH} = 4mA output buffer

  PPON(4:1)
- 3.3 V I_{OL} = 4mA bi-directional buffer

  SPISO, SPISI, SPISCK, SPICSB
- Open drain buffer

  PEWAKEB, PECREQB, SMIB
- 3.3 V oscillator interface

  XT1, XT2
- USB Classic interface

  U2DP(4:1), U2DN(4:1), RREF
- PCI Express Serdes

  PECLKP, PECLKN, PETXP, PETXN, PERXP, PERXN
- USB SuperSpeed Serdes (Serializer-Deserializer)

  U3TXDP(4:1), U3TXDN(4:1), U3RXDP(4:1), U3RXDN(4:1)

3.2 Terminology

Table 3-1. Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD10}, AV_{DD33}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a VDD pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device.

Table 3-2. Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD10}, AV_{DD33}	Indicates the voltage range for normal logic operations occur when GND = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.
Input rise time	T_{ri}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device rises from 10% to 90%.
Input fall time	T_{fi}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device falls from 90% to 10%.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.

Table 3-3. Term Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.

3.3 Absolute Maximum Ratings

Table 3-4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Units
Power supply voltage	V_{DD33}, AV_{DD33}		–0.5 to +4.6	V
	V_{DD10}		–0.5 to +1.4	V
Input voltage, 3.3 V buffer	V_I	$V_I < V_{DD33} + 0.5$ V	–0.5 to +4.6	V
Output voltage, 3.3 V buffer	V_O	$V_O < V_{DD33} + 0.5$ V	–0.5 to +4.6	V
Output current	I_O	4 mA Type	8	mA
Storage temperature	T_{stg}		–65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

3.4 Recommended Operating Ranges

Table 3-5. Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating voltage	V_{DD33}, AV_{DD33}		3.0	3.3	3.6	V
	V_{DD10}		0.9975	1.05	1.1025	V
High-level input voltage	V_{IH}		2.0		$V_{DD33}+0.3$	V
Low-level input voltage	V_{IL}		–0.3		0.8	V
Input rise time	T_{ri}	Normal Buffer	0		200	ns
		Schmitt Buffer	0		10	ms
Input fall time	T_{fi}	Normal Buffer	0		200	ns
		Schmitt Buffer	0		10	ms
Operating ambient temperature (μPD720201K8-701-BAC-A, μPD720202K8-701-BAA-A)	T_A		0		+85	°C
Operating ambient temperature (μPD720201K8-711-BAC-A, μPD720202K8-711-BAA-A)	T_A		-40		+85	°C

3.5 DC Characteristics

Table 3-6. DC Characteristics

Parameter	Symbol	Condition	Min.	Max.	Units
Off-state output current	I_{OZ}	$V_I = V_{DD33}$ or GND		±10	μA
Input leakage current	I_I	$V_I = V_{DD33}$ or GND		±10	μA
Low-level output voltage	V_{OL}	I_{OL} = 0mA		0.1	V
High-level output voltage	V_{OH}	I_{OH} = 0mA	V_{DD33}-0.1		V

Table 3-7. USB interface block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	Z_{HSDRV}		40.5	49.5	Ω
Input Levels for Low-/Full-Speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	$\lvert (D+) - (D-) \rvert$	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/Full-Speed:					
High-level output voltage	V_{OH}	RL of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	RL of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for Hi-Speed:					
Hi-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
Hi-Speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
Hi-Speed data signaling common mode voltage range	V_{HSCM}		–50	+500	mV
Hi-Speed differential input signaling level	See Figure 3-13				
Output Levels for Hi-Speed:					
Hi-Speed idle state	V_{HSOI}		–10	+10	mV
Hi-Speed data signaling high	V_{HSOH}		360	440	mV
Hi-Speed data signaling low	V_{HSOL}		–10	+10	mV
Chirp J level (differential signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (differential signal)	V_{CHIRPK}		–900	–500	mV

3.6 Pin Capacitance

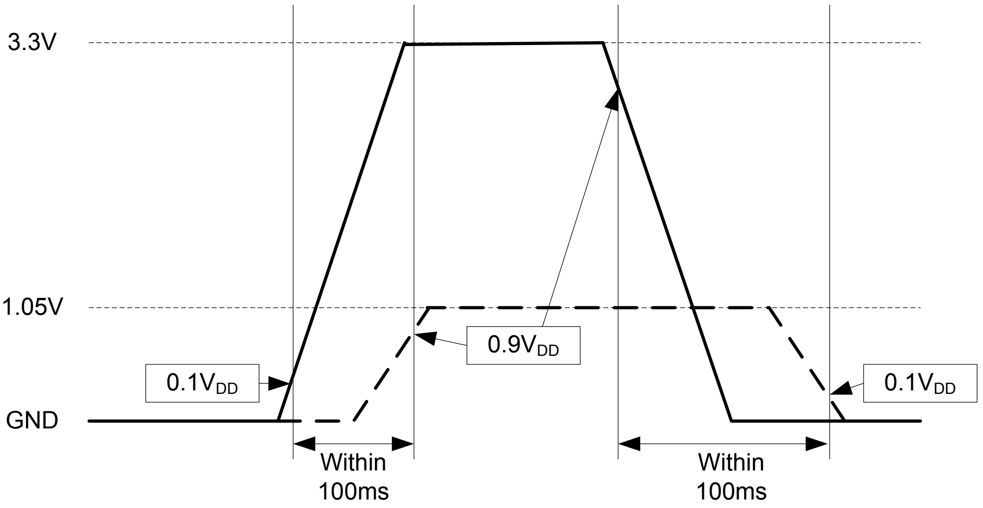
Table 3-8. Pin capacitance

Parameter	Symbol	Condition	Min.	Max.	Units
SPI Interface Pin capacitance	C_{SPI}			5	pF

3.7 Sequence for turning on or off power

It is recommended that the time difference between the start of power-supply rise (3.3V or 1.05V) and the point where both power supplies are stabilized should be within 100ms, regardless of the order of power source. A voltage of $0.1V_{DD}$ has to be raised to $0.9V_{DD}$ while the time difference is measured.

Figure 3-1. Order of Power Source



3.8 AC Characteristics

3.8.1 System Clock

Table 3-9. System clock (XT1/XT2) ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Clock frequency	F_{CLK}	Crystal	–100 ppm	24	+100 ppm	MHz
Clock duty cycle	T_{DUTY}		40	50	60	%

Remark Required accuracy of crystal or oscillator block includes initial frequency accuracy, the spread of Crystal capacitor loading, supply voltage, temperature and aging, etc.

3.8.2 PCI Express Reference Clock

Table 3-10. PCI Express Interface - Reference Clock (PECLKP and PECLKN) Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Rising Edge Rate	T_{RISE}	See Figure 3-5	0.6	4.0	V/ns
Falling Edge Rate	T_{FALL}	See Figure 3-5	0.6	4.0	V/ns
Differential Input High Voltage	V_{IH}	See Figure 3-8	+150		mV
Differential Input Low Voltage	V_{IL}	See Figure 3-8		–150	mV
Absolute crossing point voltage	V_{CROSS}	See Figure 3-3	+250	+550	mV
Variation of V_{CROSS} over all rising clock edge	$V_{CROSS\ DELTA}$	See Figure 3-4		+140	mV
Ring-back Voltage Margin	V_{RB}	See Figure 3-8	–100	+100	mV
Time before V_{RB} is allowed	T_{STABLE}	See Figure 3-8	500		ps
Average Clock Period Accuracy	$T_{PERIOD\ AVG}$		–300	+2800	ppm
Absolute Period (including Jitter and Spread Spectrum)	$T_{PERIOD\ ABS}$		9.847	10.203	ns
Cycle to Cycle Jitter	$V_{CCJITTER}$			150	ps
Absolute Max input voltage	V_{MAX}	See Figure 3-3		+1.15	V
Absolute Min input voltage	V_{MIN}	See Figure 3-3		–0.3	V
Duty Cycle		See Figure 3-6	40	60	%
Rising edge rate (PECLKP) to falling edge rate (PECLKN) matching		See Figure 3-7		20	%
Clock source DC impedance	Z_{C-DC}	See Figure 3-2	40	60	Ω

Figure 3-2. PCI Express Reference Clock System Measurement Point and Loading

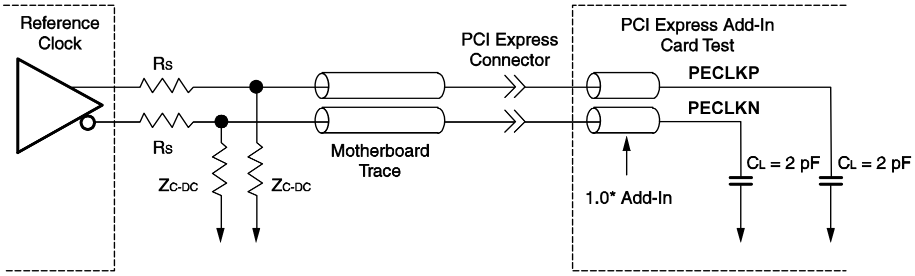


Figure 3-3. PCI Express Single-Ended Measurement Points for Absolute Cross Point and Swing

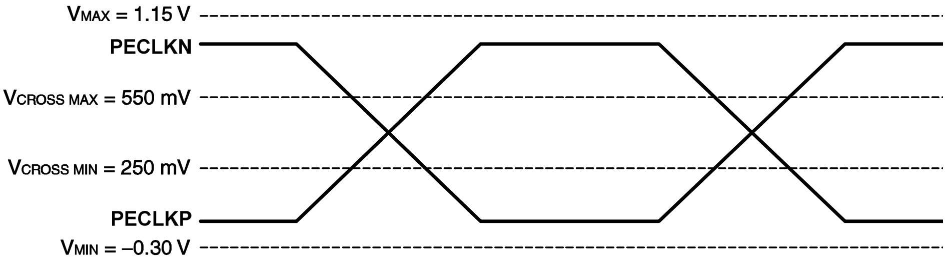


Figure 3-4. PCI Express Single-Ended Measurement Points for Delta Cross Point

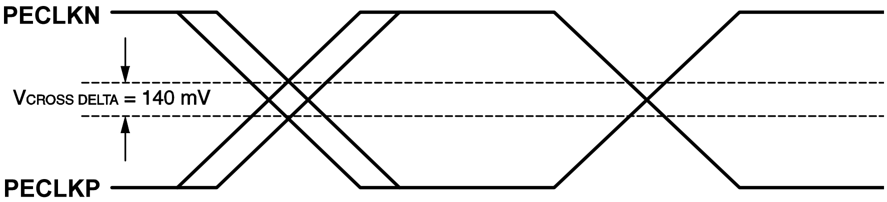


Figure 3-5. PCI Express Single-Ended Measurement Points for Rise and Fall Time Matching

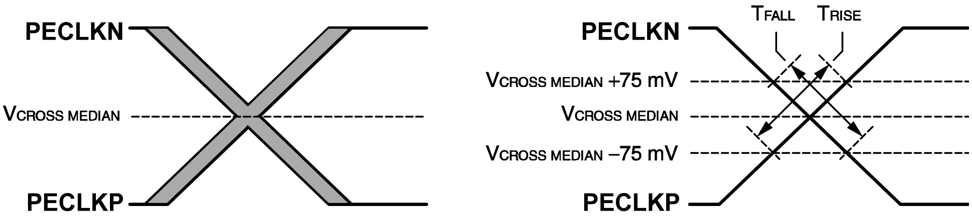


Figure 3-6. PCI Express Differential Measurement Points for Duty Cycle and Period

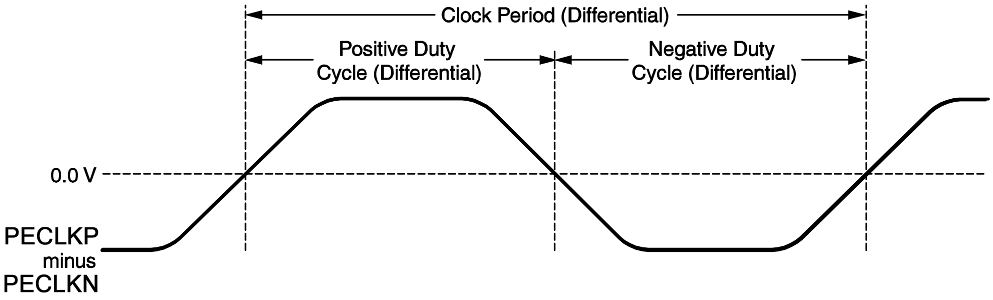


Figure 3-7. PCI Express Differential Measurement Points for Rise and Fall Time

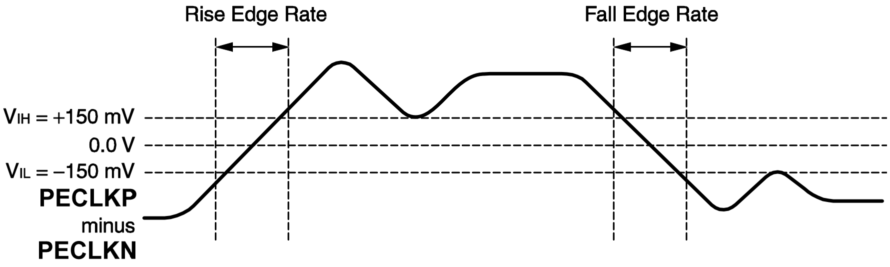
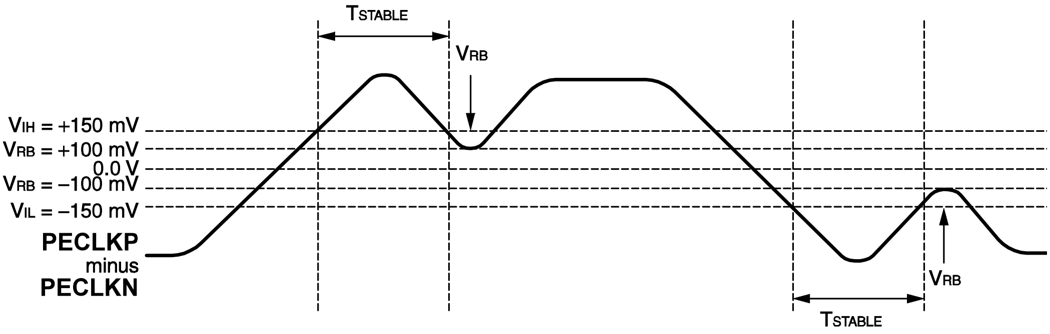


Figure 3-8. PCI Express Differential Measurement Points for Ring-back



3.8.3 Reset

Table 3-11. Power on Reset (PONRSTB) Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Power on reset time	T_{PONRST}	See Figure 3-9	1		ms

Remarks 1. There is no order to power-on of V_{DD33}, AV_{DD33}, AV_{DD33} and V_{DD10}.

2. All power sources should be stable within 100 ms from the fastest rising edge of power sources.

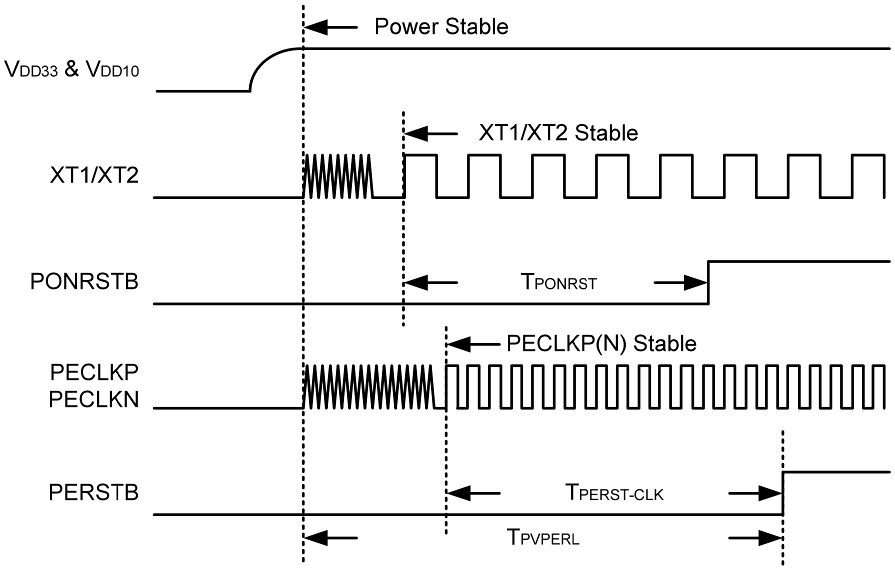
3. PONRSTB shall be de-asserted after all power sources and the system clock become stable.

4. PONRSTB shall be de-asserted before de-asserting PERSTB.

Table 3-12. PCI Express Interface - PERSTB Signal Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Power stable to PERSTB inactive	T_{PVPERL}	See Figure 3-9	100		ms
PECLKP/PECLKN stable before PERSTB inactive	$T_{PERST-CLK}$	See Figure 3-9	100		μs

Figure 3-9. Power Up and Reset



Remark As a power saving feature, the μPD720201 / μPD720202 stops XT1/XT2 oscillation whenever PERSTB is asserted (low) while PONRSTB is inactive (high). XT1/XT2 oscillation does not stop while PONRSTB is asserted (low).

3.8.4 PCI Express CLKREQ#

Table 3-13. PCI Express Interface – Power-Up and PECREQB Signal Timings

Parameter	Symbol	Condition	Min.	Max.	Units
PONRSTB inactive to PECREQB Output active	T_{PVCRL}	See Figure 3-10		1	μs

Table 3-14. PCI Express Interface – PECREQB Clock Control Timings

Parameter	Symbol	Condition	Min.	Max.	Units
PECREQB de-asserted high to clock parked	T_{CRHOFF}	See Figure 3-11	0		ns
PECREQB asserted low to clock active	T_{CRLON}	See Figure 3-11		400	ns

Figure 3-10. PCI Express Power-Up PECREQB Timing

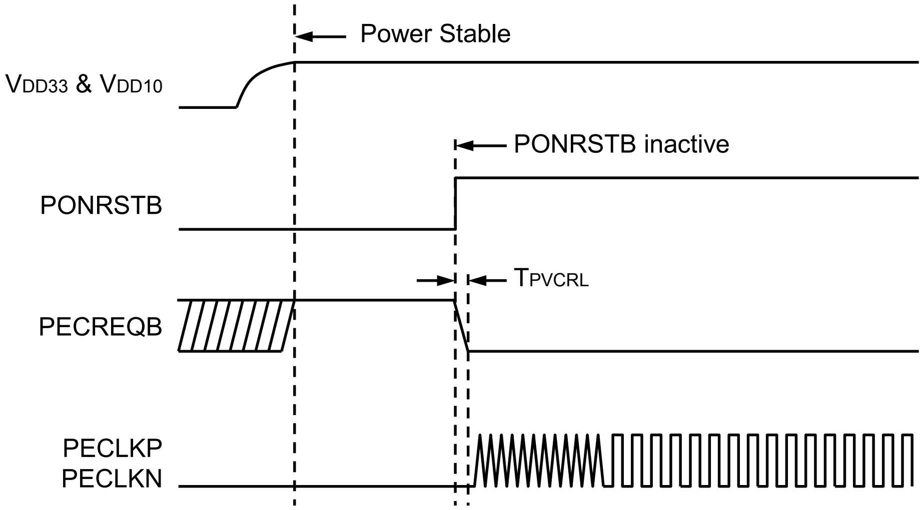
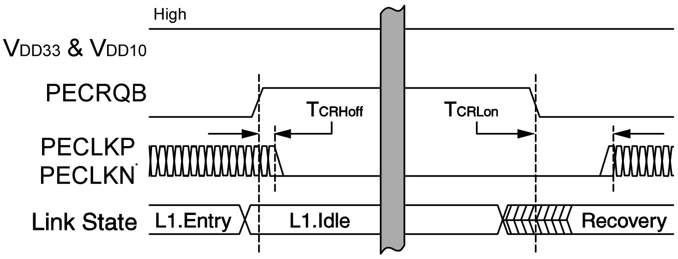


Figure 3-11. PCI Express PECREQB Clock Control Timing



3.8.5 PCI Express Interface – Differential Transmitter (TX) Specifications

(Refer to PCI Express Base Specification Revision 2.0 for more information)

Table 3-15. PCI Express Interface – Differential Transmitter (TX) Specifications

(1/2)

Parameter	Symbol	2.5GT/s	5.0GT/S.	Units
Unit Interval	UI	399.88(min) 400.12(max)	199.94(min) 200.06(max)	ps
Differential Peak to Peak(p-p) Tx voltage swing	$V_{\text{TX-DIFFp-p}}$	0.8(min) 1.2(max)	0.8(min) 1.2(max)	V
Tx de-emphasis level ratio	$V_{\text{TX-DE-RATIO-3.5dB}}$	3.0(min) 4.0(max)	3.0(min) 4.0(max)	dB
Tx de-emphasis level ratio	$V_{\text{TX-DE-RATIO-6dB}}$	Not specified	5.5(min) 6.5(max)	dB
Instantaneous lone pulse width	$T_{\text{MIN-PULSE}}$	Not specified	0.9(min)	UI
Transmitter Eye including all jitter sources	$T_{\text{TX-EYE}}$	0.75(min)	0.75(min)	UI
Maximum time between the jitter median and max deviation from the median	$T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$	0.125(max)	Not specified	UI
Tx deterministic jitter >1.5MHz	$T_{\text{TX-HF-DJ-DD}}$	Not specified	0.15(max)	UI
Tx RMS jitter > 1.5MHz	$T_{\text{TX-LF-RMS}}$	Not specified	3.0	ps RMS
Transmitter rise and fall time	$T_{\text{TX-RISE-FALL}}$	0.125(min)	0.15(max)	UI
Tx rise/fall mismatch	$T_{\text{RF-MISMATCH}}$	Not specified	0.1(max)	UI
Maximum Tx PLL bandwidth	$B_{\text{WTX-PLL}}$	22(max)	16(max)	MHz
Minimum Tx PLL BW for 3dB peaking	$B_{\text{WTX-PLL-LO-3DB}}$	1.5(min)	8(min)	MHz
Minimum Tx PLL BW for 1dB peaking	$B_{\text{WTX-PLL-LO-1DB}}$	Not specified	5(min)	MHz
Tx PLL peaking with 8MHz min BW	$P_{\text{KGTX-PLL1}}$	Not specified	3.0(max)	dB
Tx PLL peaking with 5MHz min BW	$P_{\text{KGTX-PLL2}}$	Not specified	1.0(max)	dB
Tx package plus Si differential return loss	$R_{\text{LTX-DIFF}}$	10(min)	10(min) for 0.05 – 1.25GHz 8(min) for 1.25 – 2.5GHz	dB
Tx package plus Si common mode return loss	$R_{\text{LTX-CM}}$	6(min)	6(min)	dB
DC differential Tx impedance	$Z_{\text{TX-DIFF-DC}}$	80(min) 120(max)	120(max)	Ω

(2/2)

Parameter	Symbol	2.5GT/s	5.0GT/S.	Units
Tx AC common mode voltage (5GT/s)	$V_{TX-CM-AC-PP}$	Not specified	100(max)	mVPP
Tx AC common mode voltage (2.5GT/s)	$V_{TX-CM-AC-P}$	20	Not specifed	mV
Transmitter short-circuit current limit	$I_{TX-SHORT}$	90(max)	90(max)	mA
Transmitter DC common-mode voltage	$V_{TX-DC-CM}$	0(min) 3.6(max)	0(min) 3.6(max)	V
Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0(min) 100(max)	0(min) 100(max)	mV
Absolute Delta of DC Common Mode Voltage between PETXP and PETXN	$V_{TX-CM-DC-LINE-DELTA}$	0(min) 25(max)	0(min) 25(max)	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0(min) 20(max)	0(min) 20(max)	mV
DC Electrical Idle Differential Output Voltage	$V_{TX-IDLE-DIFF-DC}$	Not specified	0(min) 5(max)	mV
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$	600(max)	600(max)	mV
Minimum time spent in Electrical Idle	$T_{TX-IDLE-MIN}$	20(min)	20(min)	ns
Maximum time to transition to a valid Electrical Idle after sending an EIOS	$T_{TX-IDLE-SET-TO-IDLE}$	8(max)	8(max)	ns
Maximum time to transition to valid diff signaling after leaving Electrical Idle	$T_{TX-IDLE-TO-DIFF-DATA}$	8(max)	8(max)	ns
Crosslink random timeout	$T_{CROSSLINK}$	1.0(max)	1.0(max)	ns
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	500ps + 2UI(max)	500ps + 4UI(max)	ps
AC Coupling Capacitor	C_{TX}	75(min) 200(max)	75(min) 200(max)	nF

3.8.6 PCI Express Interface – Differential Receiver (RX) Specifications

(Refer to PCI Express Base Specification Revision 2.0 for more information)

Table 3-16. PCI Express Interface – Differential Receiver (RX) Specifications

(1/2)

Parameter	Symbol	2.5GT/s	5.0GT/S.	Units
Unit Interval	UI	399.88(min) 400.12(max)	199.94(min) 200.06(max)	ps
Differential Rx peak-peak voltage for common Reference clock Rx architecture	$V_{\text{RX-DIFF-PP-CC}}$	0.175(min) 1.2(max)	0.120(min) 1.2(max)	V
Differential Rx peak-peak voltage for data clocked Rx architecture	$V_{\text{RX-DIFF-PP-DC}}$	0.175(min) 1.2(max)	0.100(min) 1.2(max)	V
Receiver eye time opening	$t_{\text{RX-EYE}}$	0.40(min)	Not specified	UI
Max Rx inherent timing error	$t_{\text{RX-TJ-CC}}$	Not specified	0.40(max)	UI
Max Rx inherent timing error	$t_{\text{RX-TJ-DC}}$	Not specified	0.34(max)	UI
Max Rx inherent deterministic timing error	$t_{\text{RX-DJ-DD-CC}}$	Not specified	0.30(max)	UI
Max Rx inherent deterministic timing error	$t_{\text{RX-DJ-DD-DC}}$	Not specified	0.24(max)	UI
Max time delta between median and deviation from median	$t_{\text{RX-EYE-MEDIAN-to-MAX-JITTER}}$	0.3(max)	Not specified	UI
Minimum width pulse at Rx	$t_{\text{RX-MIN-PULSE}}$	Not specified	0.6(min)	UI
Min/max pulse voltage on consecutive UI	$t_{\text{RX-MAX-MIN-RATIO}}$	Not specified	5(max)	-
Maximum Rx PLL bandwidth	$B_{\text{WRX-PLL-HI}}$	22(max)	16(max)	MHz
Minimum Rx PLL BW for 3dB peaking	$B_{\text{WRX-PLL-LO-3DB}}$	1.5(min)	8(min)	MHz
Minimum Rx PLL BW for 1dB peaking	$B_{\text{WRX-PLL-LO-1DB}}$	Not specified	5(min)	MHz
Rx PLL peaking with 8 MHz min BW	$P_{\text{KGRX-PLL1}}$	Not specified	3.0	dB
Rx PLL peaking with 5MHz min BW	$P_{\text{KGRX-PLL2}}$	Not specified	1.0	dB
Rx package plus Si differential return loss	$R_{\text{LRX-DIFF}}$	10(min)	10(min) for 0.05 – 1.25GHz 8(min) for 1.25 – 2.5GHz	dB
Common mode Rx return loss	$R_{\text{LRX-CM}}$	6(min)	6(min)	dB
Receiver DC single ended impedance	$Z_{\text{RX-DC}}$	40(min) 60(max)	40(min) 60(max)	Ω
DC differential impedance	$Z_{\text{RX-DIFF-DC}}$	80(min) 120(max)	Not specified	Ω

(2/2)

Parameter	Symbol	2.5GT/s	5.0GT/S.	Units
Rx AC common mode voltage	$V_{RX-CM-AC-P}$	150(max)	150(max)	mVP
DC input CM input Impedance for V>0 during Reset or power down	$Z_{RX-HIGH-IMP-DC-POS}$	50k(min)	50k(min)	Ω
DC input CM input Impedance for V<0 during Reset or power down	$Z_{RX-HIGH-IMP-DC-NEG}$	1.0k(min)	1.0k(min)	Ω
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65(min) 175(max)	65(min) 175(max)	mV
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$t_{RX-IDLE-DET-DIFF-ENTERTIME}$	10(max)	10(max)	ms
Lane to Lane skew	$L_{RX-SKEW}$	20(max)	8(max)	ns

3.8.7 USB3.0 SuperSpeed Interface – Differential Transmitter (TX) Specifications

(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Table 3-17. Transmitter Normative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Differential p-p Tx voltage swing	$V_{TX\text{-}DIFF\text{-}PP}$	0.8	1.2	V
Tx de-emphasis	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	4.0	dB
DC differential impedance	$R_{TX\text{-}DIFF\text{-}DC}$	72	120	Ω
The amount of voltage change allowed during Receiver Detection	$V_{TX\text{-}RCV\text{-}DETECT}$		0.6	V
AC Coupling Capacitor	$C_{AC\text{-}COUPLING}$	75	200	nF
Maximum slew rate	$t_{CDR\text{-}SLEW\text{-}MAX}$		10	ms/s

Table 3-18. Transmitter Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Deterministic min pulse	$t_{MIN\text{-}PULSE\text{-}Dj}$	0.96		UI
Tx min pulse	$t_{MIN\text{-}PULSE\text{-}Tj}$	0.90		UI
Transmitter Eye	$t_{TX\text{-}EYE}$	0.625		UI
Tx deterministic jitter	$t_{TX\text{-}DJ\text{-}DD}$		0.205	UI
Tx input capacitance for return loss	$C_{TX\text{-}PARASITIC}$		1.25	pF
Transmitter DC common mode impedance	$R_{TX\text{-}DC}$	18	30	Ω
Transmitter short-circuit current limit	$I_{TX\text{-}SHORT}$		60	mA
Transmitter DC common-mode voltage	$V_{TX\text{-}DC\text{-}CM}$	0	2.2	V
Tx AC common mode voltage	$V_{TX\text{-}CM\text{-}AC\text{-}PP\text{-}ACTIVE}$		100	mVp-p
Absolute DC Common Mode Voltage between U1 and U0	$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$		200	mV
Electrical Idle Differential Peak- Peak Output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}AC\text{-}pp}$	0	10	mV
DC Electrical Idle Differential Output Voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0	10	mV

3.8.8 USB3.0 SuperSpeed Interface – Differential Receiver (RX) Specifications

(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Table 3-19. Receiver Normative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Receiver DC common mode impedance	R_{RX-DC}	18	30	Ω
DC differential impedance	$R_{RX-DIFF-DC}$	72	120	Ω
DC Input CM Input Impedance for V>0 during Reset of Power down	$Z_{RX-HIGH-IMP-DC-POS}$	25k		Ω
LFPS Detect Threshold	$V_{RX-LFPS-DET-DIFF-p-p}$	100	300	mV

Table 3-20. Receiver Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Differential Rx peak-to-peak voltage	$V_{RX-DIFF-PP-POST-EQ}$	30		mV
Max Rx inherent timing error	T_{RX-Tj}		0.45	UI
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD}$		0.285	UI
Rx input capacitance for return loss	$C_{RX-PARASITIC}$		1.1	pF
Rx AC common mode voltage	$V_{RX-CM-AC-P}$		150	mVPeak
Rx AC common mode voltage during the U1 to U0 transition	$V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$		200	mVPeak

3.8.9 USB2.0 interface

(Refer to Universal Serial Bus Specification Revision 2.0 for more information)

Table 3-21. Low-Speed Source Electrical Characteristics

Parameter	Symbol	Min	Max	Units
Driver Characteristics:				
Transition Time:				
Rise Time	T_{LR}	75	300	ns
Fall Time	T_{LF}	75	300	ns
Rise and Fall Time Matching	T_{LRFM}	80	125	%
Clock Timings:				
Low-Speed Data Rate	$T_{LDRATHS}$	1.49925	1.50075	Mb/s
Low-Speed Data Timing:				
Source Jitter for Differential Transition to SE0 Transition	T_{LDEOP}	–40	100	ns
Source Jitter total (including frequency tolerance):				
To Next Transition	T_{DDJ1}	–25	25	ns
For Paired Transitions	T_{DDJ2}	–14	14	ns
Differential Receiver Jitter:				
To Next Transition	T_{UJR1}	–152	152	ns
For Paired Transitions	T_{UJR2}	–200	200	ns
Source SE0 interval of EOP	T_{LEOPT}	1.25	1.50	μs
Receiver SE0 interval of EOP	T_{LEOPR}	670		ns
Width of SE0 interval during differential transition	T_{LST}		210	ns

Table 3-22. Full-Speed Source Electrical Characteristics

Parameter	Symbol	Min	Max	Units
Driver Characteristics:				
Rise Time	T_{FR}	4	20	ns
Fall Time	T_{FF}	4	20	ns
Differential Rise and Fall Time Matching	T_{FRFM}	90	111.11	%
Clock Timings:				
Full-Speed Data Rate	$T_{FDRATHS}$	11.9940	12.0060	Mb/s
Frame Interval	T_{FRAME}	0.9995	1.0005	ms
Consecutive Frame Interval Jitter	T_{RFI}		42	ns
Full-Speed Data Timing:				
Source Jitter for Differential Transition to SE0 Transition	T_{FDEOP}	–2	5	ns
Source Jitter total (including frequency tolerance):				
To Next Transition	T_{DJ1}	–3.5	3.5	ns
For Paired Transitions	T_{DJ2}	–4	4	ns
Receiver Jitter:				
To Next Transition	T_{JR1}	–18.5	18.5	ns
For Paired Transitions	T_{JR2}	–9	9	ns
Source SE0 interval of EOP	T_{FEOPT}	160	175	ns
Receiver SE0 interval of EOP	T_{FEOPR}	82		ns
Width of SE0 interval during differential transition	T_{FST}		14	ns

Table 3-23. Hi-Speed Source Electrical Characteristics

Parameter	Symbol	Min	Max	Units
Driver Characteristics:				
Rise Time (10% - 90%)	T_{HSR}	500		ps
Fall Time (10% - 90%)	T_{HSF}	500		ps
Driver waveform requirements	See Figure 3-15			
Clock Timings:				
Hi-Speed Data Rate	T_{HSDRAT}	497.760	480.240	Mb/s
Microframe Interval	$T_{HSFRAME}$	124.9375	125.0625	μs
Consecutive Microframe Interval Difference	T_{HSRFI}		4 Hi-Speed bit times	
Hi-Speed Data Timing:				
Data source jitter	See Figure 3-15			
Receiver jitter tolerance	See Figure 3-13			

Table 3-24. Hub Event Timings

Parameter	Symbol	Min	Max	Units
Time to detect a downstream facing port connect event	T_{DCNN}	2.5	2000	μs
Time to detect a disconnect event at a hub's downstream facing port	T_{DDIS}	2	2.5	μs
Duration of driving resume to a downstream port	T_{DRSMDN}	20		ms
Time from detecting downstream resume to rebroadcast	T_{URSM}		1.0	ms
Inter-packet delay for packets traveling in same direction	$T_{HSIPDSD}$	88		Bit times
Inter-packet delay for packets traveling in opposite direction	$T_{HSIPDOD}$	8		Bit times
Inter-packet delay for root hub response for Hi-Speed	$T_{HSRSPIPD1}$		192	Bit times
Time for which a Chirp J or Chirp K must be continuously detected by hub during Reset handshake	T_{FILT}	2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	T_{DCHBIT}		100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	T_{DCHBIT}	40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	T_{DCHSE0}	100	500	μs

Figure 3-12. Differential Input Sensitivity Range for Low-/Full-Speed

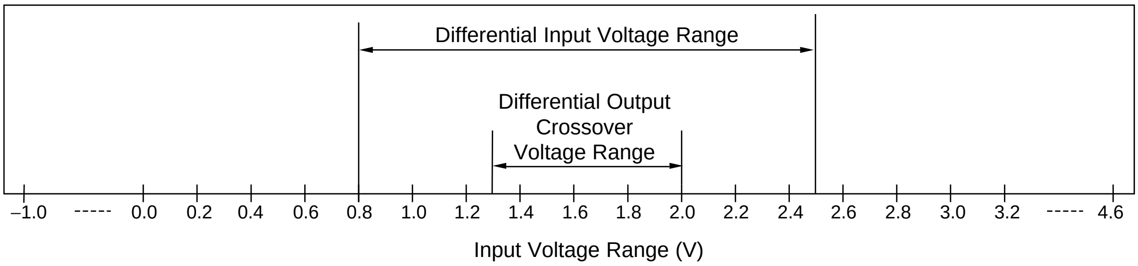


Figure 3-13. Receiver Sensitivity for Transceiver at U2DP/U2DM

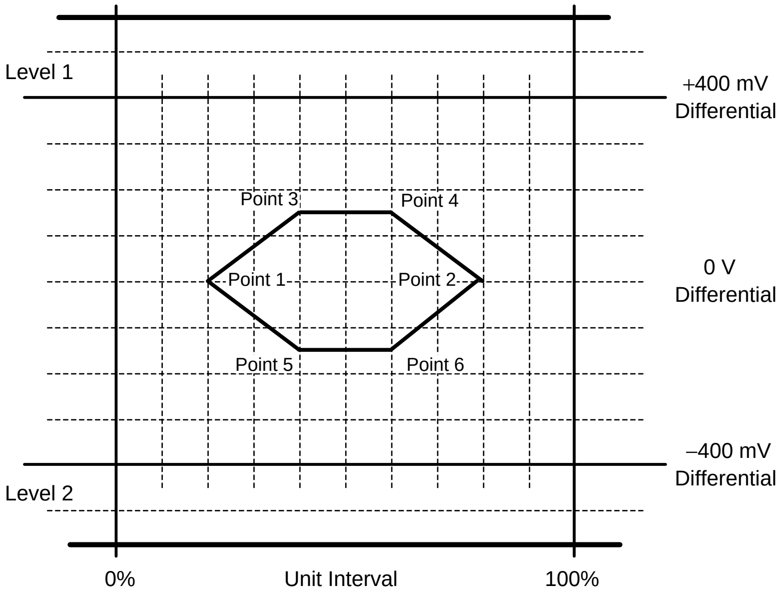


Figure 3-14. Receiver Measurement Fixtures

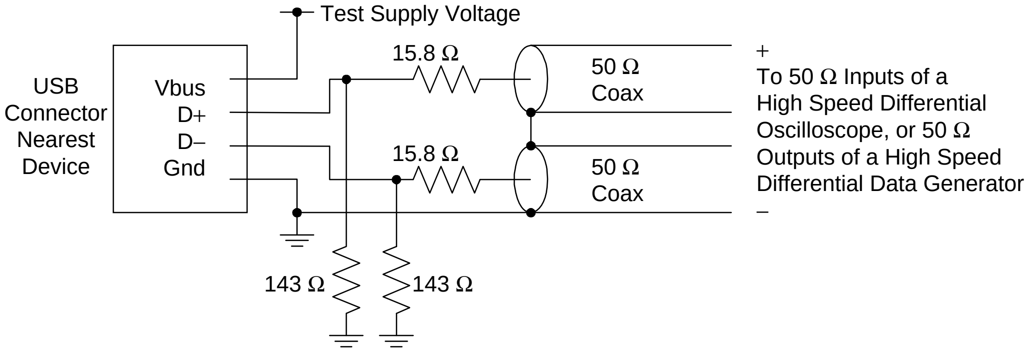


Figure 3-15. Transmit Waveform for Transceiver at U2DP/U2DM

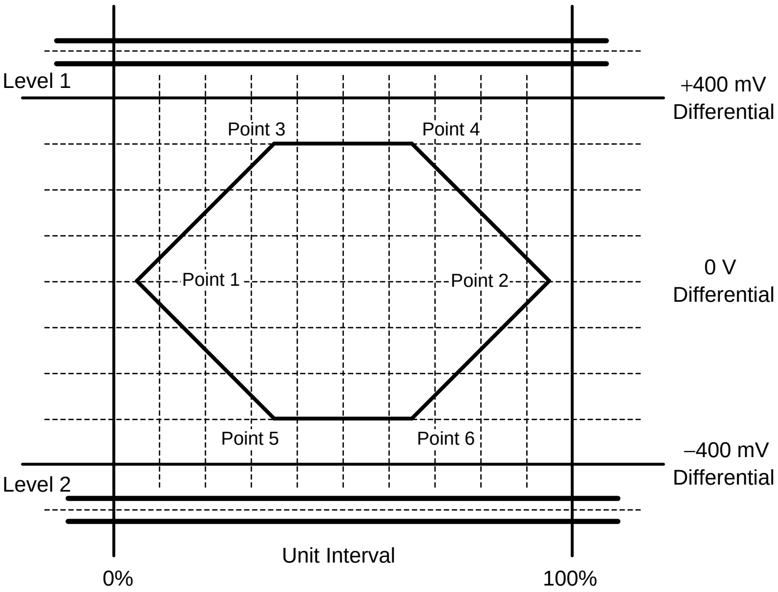


Figure 3-16. Transmitter Measurement Fixtures

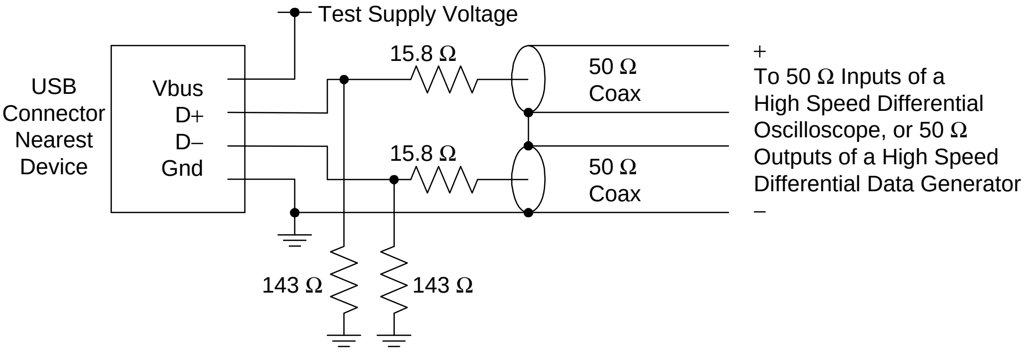


Figure 3-17. Differential Data Jitter for Low-/Full-Speed

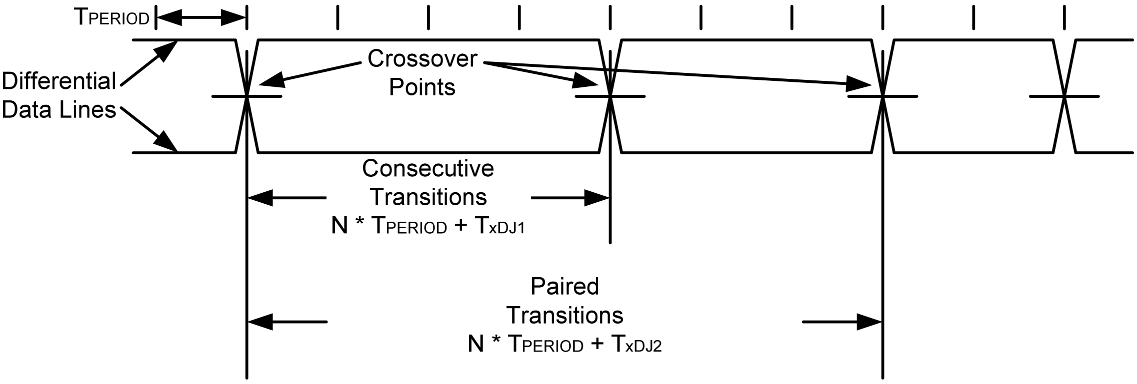


Figure 3-18. Differential-to-EOP Transition Skew and EOP Width for Low-/Full-Speed

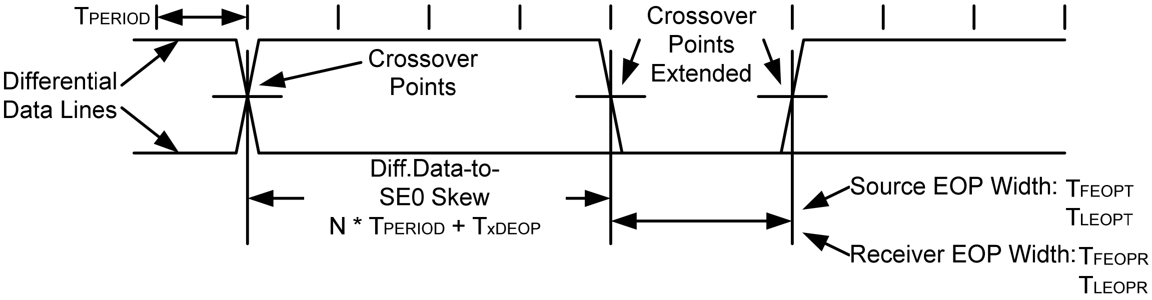
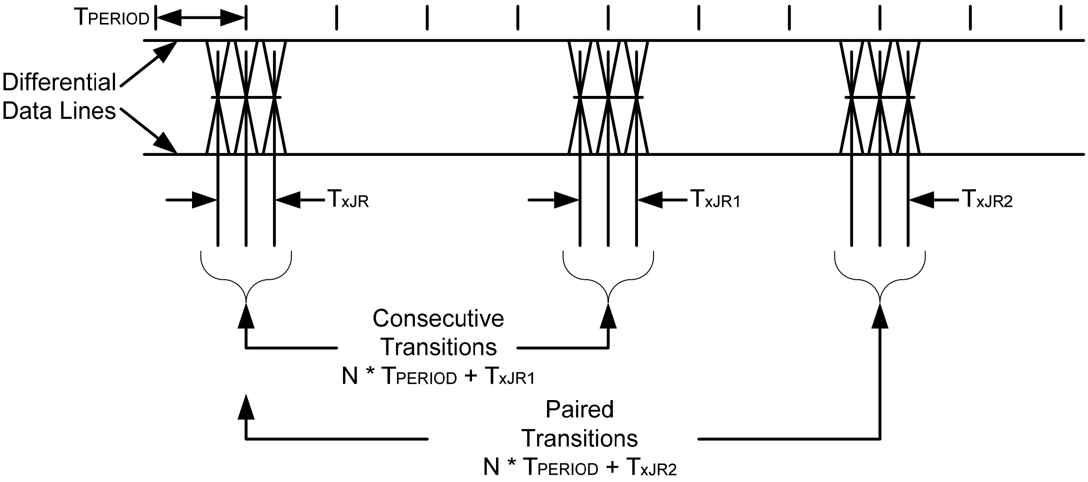


Figure 3-19. Receiver Jitter Tolerance for Low-/Full-Speed



3.8.10 SPI Type Serial ROM Interface

Table 3-25. SPI Type Serial ROM Interface Signals Timing (SPI Mode 0)

Parameter	Symbol	Min.	Max.	Units
SPISCK Clock Frequency		1	20	MHz
Clock pulses width Low	t_{SCLLOW}	25		ns
Clock pulses width high	$t_{SCLHIGH}$	25		ns
SPICSB disable time	t_{SCSDIS}	100		ns
SPICSB setup time	t_{SCSSU}	25		ns
SPICSB hold time	t_{SCSH}	20		ns
SPISI setup time to SPISCK rising edge	t_{SDWSU}	6		ns
SPISI hold time from SPISCK rising edge	t_{SDWH}	6		ns
SPISO validate time from SPISCK falling edge	$t_{SDRVALID}$		25	ns
SPISO hold time from SPISCK falling edge	t_{SDRH}	0		ns
SPISO pull-up time from SPICSB disabled **(Note)**	t_{SRDET}		170	ns

Note “SPISO disable time from SPICSB disabled [t_{SDRDIS}]” is expanded including “SPISO pull-up time [t_{SRDET}]” as of Rev5.00. This specification must be met only if μPD720201 and μPD720202 aborts firmware loading by PCIe reset.

Figure 3-20. SPI Type Serial ROM Signal Timing

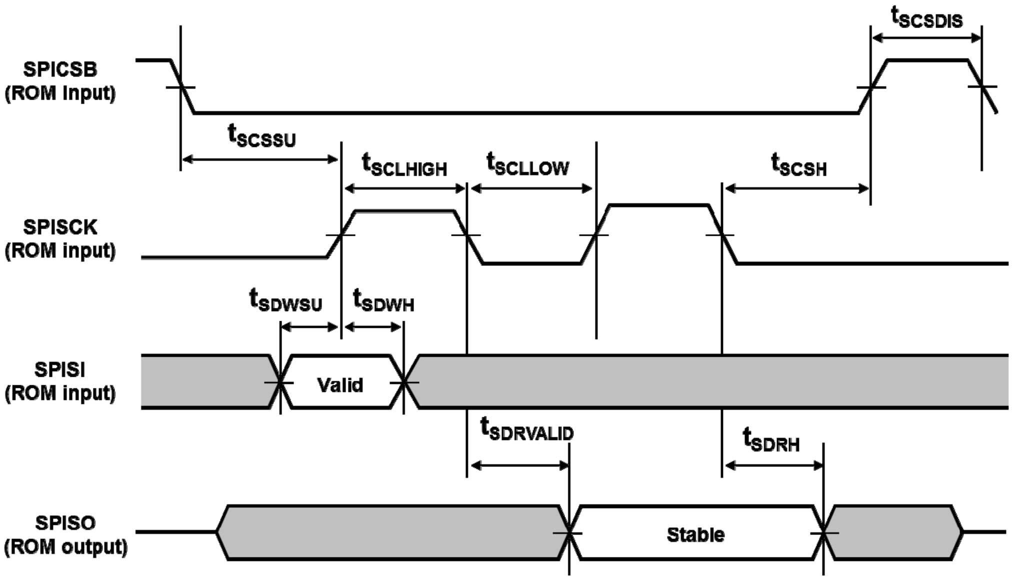
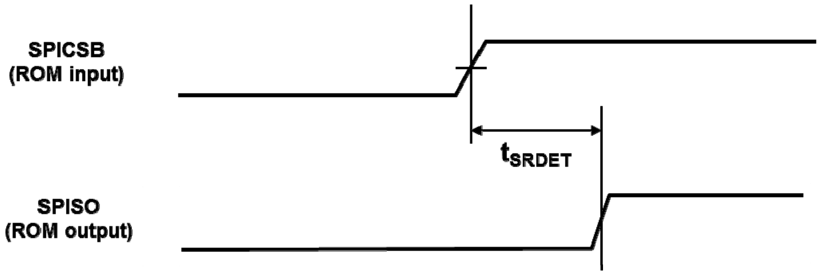


Figure 3-21. SPISO Pull-up Timing from SPICSB disabled

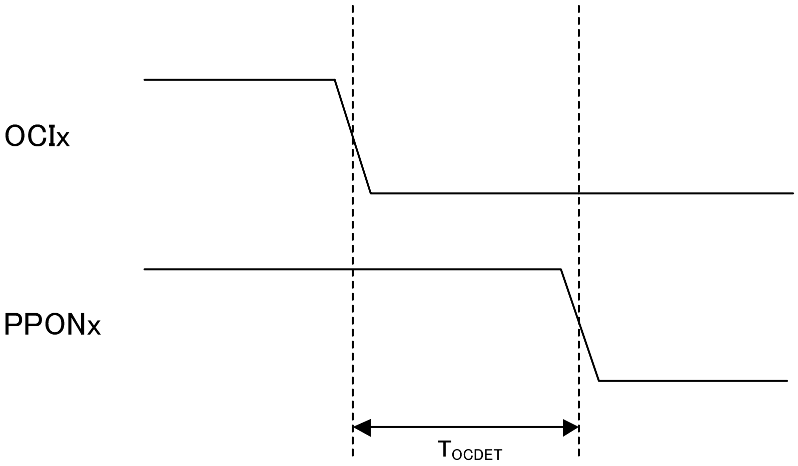


<R> 3.8.11 Overcurrent

Table 3-26. Overcurrent Detect Timing

Parameter	Symbol	Min.	Max.	Units
PPON de-assert time from asserting OCIx	T_{OCDET}	5	25	ms

Figure 3-22. Overcurrent Detect Timing



3.9 Power Consumption

Table 3-27. Power Consumption of μPD720201

Parameter	Device connection	Condition	VDD10 line	VDD33 line	AVDD33 line	Units
Power Consumption	No device	There is no device on the ports under the L1 condition.	10	0.4	1.0	mA
		There is no device on the ports under the L0 condition.	150	3	22	mA
	1 device	Only one device is connected on the port.				
		Low-Speed data transfer on the port.	30	3	10	mA
		Full-Speed data transfer on the port.	140	3	22	mA
		Hi-Speed data transfer on the port.	150	35	22	mA
		SuperSpeed transfer on the port.	430	3	32	mA
	2 devices	Two devices are connected on the ports.				
		Low-Speed data transfer on the both ports.	40	3	10	mA
		Full-Speed data transfer on the both ports.	160	4	22	mA
		Hi-Speed data transfer on the both ports.	150	43	22	mA
		SuperSpeed transfer on the both ports.	520	3	32	mA
	3 devices	Three devices are connected on the ports.				
		Low-Speed data transfer on the three ports.	40	3	10	mA
		Full-Speed data transfer on the three ports.	170	5	22	mA
		Hi-Speed data transfer on the three ports.	150	48	22	mA
		SuperSpeed transfer on the three ports.	610	3	32	mA
	4 devices	Four devices are connected on the ports.				
		Low-Speed data transfer on the four ports.	40	3	11	mA
		Full-Speed data transfer on the four ports.	180	6	22	mA
		Hi-Speed data transfer on the four ports.	150	55	22	mA
		SuperSpeed transfer on the four ports.	700	3	32	mA
	4 SS hubs with SS and HS devices	Four SuperSpeed hub are connected on the all ports under SS and HS data transfer.	710	57	32	mA
	No device (D3-cold)	Power consumption during system sleep condition. (Wake On Connect, Wake On Disconnect and Wake On Over-current are disabled.)	0.9	0.3	0.1	mA
		Power consumption during system sleep condition. (Wake On Connect, Wake On Disconnect and/or Wake On Over-current are enabled.)	3.4	0.3	1.0	mA
	LS device (D3-cold)	Power consumption during system sleep condition with one LS device enabling the remote wakeup function.	2.9	0.3	0.1	mA

Typical condition (T_A = 25°C, V_{DD33} = 3.3 V, V_{DD10} = 1.05 V), operating PCI Express Gen2 system.

Table 3-28. Power Consumption of μPD720202

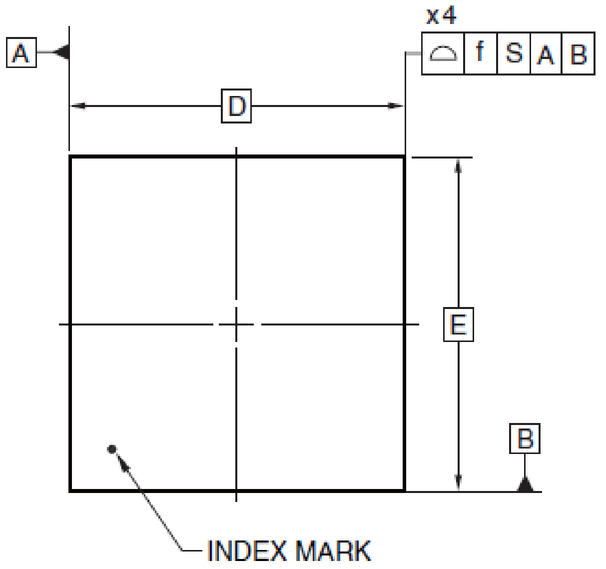
Parameter	Device connection	Condition	VDD10 line	VDD33 line	AVDD33 line	Units
Power Consumption	No device	There is no device on the ports under the L1 condition.	8	0.2	1.0	mA
		There is no device on the ports under the L0 condition.	150	3	22	mA
	1 device	Only one device is connected on the port.				
		Low-Speed data transfer on the port.	30	2	10	mA
		Full-Speed data transfer on the port.	130	3	22	mA
		Hi-Speed data transfer on the port.	140	35	22	mA
		SuperSpeed transfer on the port.	360	2	32	mA
	2 devices	Two devices are connected on the ports.				
		Low-Speed data transfer on the both ports.	30	2	11	mA
		Full-Speed data transfer on the both ports.	150	3	22	mA
		Hi-Speed data transfer on the both ports.	140	43	22	mA
		SuperSpeed transfer on the both ports.	450	2	32	mA
	2 SS hubs with SS and HS devices	Two SuperSpeed hub are connected on the both ports under SS and HS data transfer.	460	42	32	mA
	No device (D3-cold)	Power consumption during system sleep condition. (Wake On Connect, Wake On Disconnect and Wake On Over-current are disabled.)	0.7	0.1	0.1	mA
		Power consumption during system sleep condition. (Wake On Connect, Wake On Disconnect and/or Wake On Over-current are enabled.)	2.2	0.1	0.9	mA
	LS device (D3-cold)	Power consumption during system sleep condition with one LS device enabling the remote wakeup function.	1.8	0.1	0.1	mA

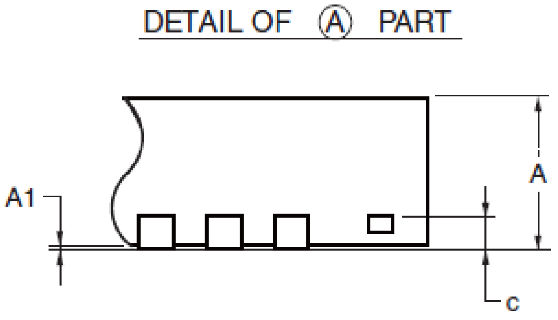
Typical condition (T_A = 25°C, V_{DD33} = 3.3 V, V_{DD10} = 1.05 V), operating PCI Express Gen2 system.

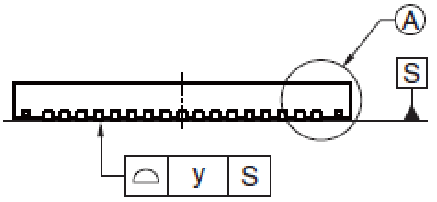
4. PACKAGE DRAWINGS

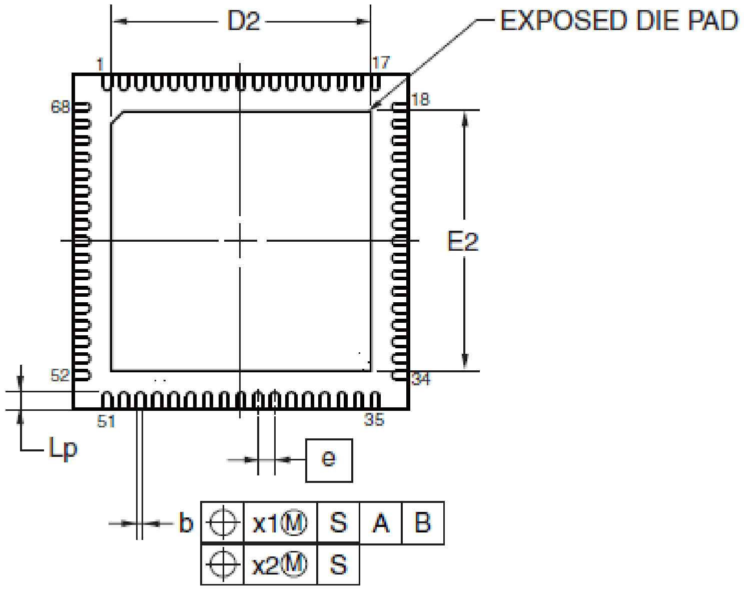
- *μ*PD720201K8-701-BAC-A
- *μ*PD720201K8-711-BAC-A

68-PIN QFN (8x8)







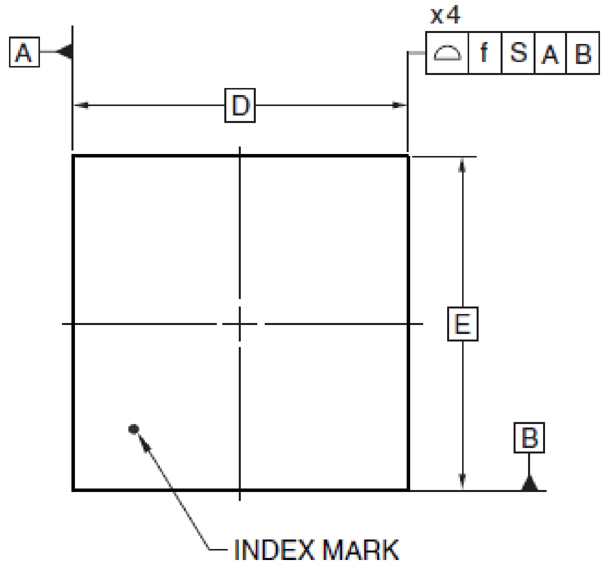


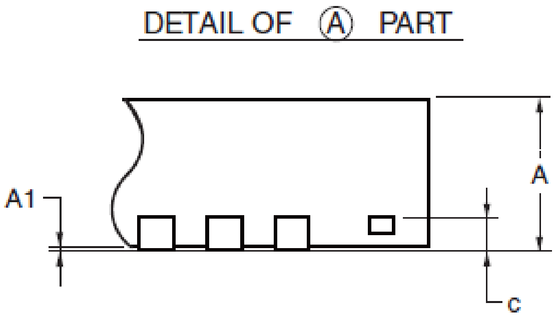
(UNIT:mm)

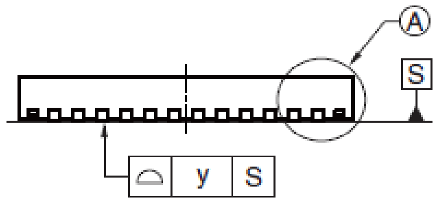
ITEM	DIMENSIONS
D	8.00
E	8.00
A	0.90 MAX.
A1	0.05 MAX.
b	0.20±0.05
c	0.20
e	0.40
f	0.10
Lp	0.40±0.05
x1	0.07
x2	0.05
y	0.08
D2	6.20
E2	6.20

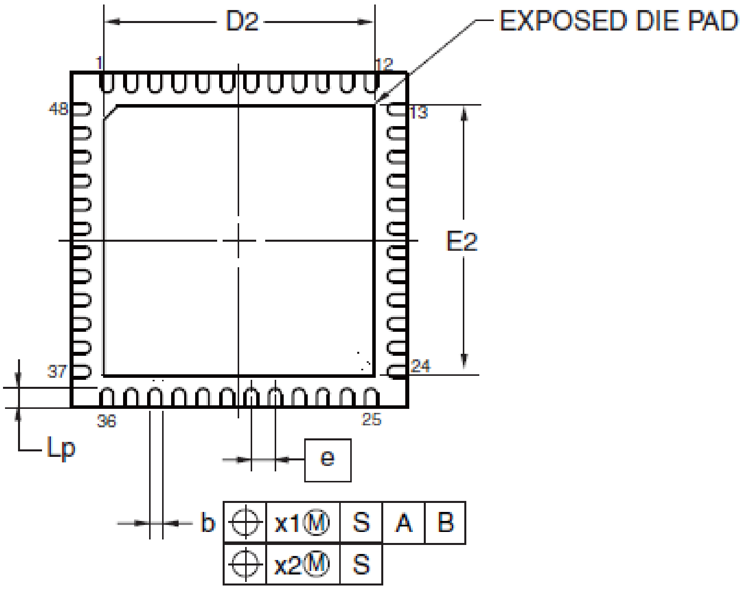
- μPD720202K8-701-BAA-A
- μPD720202K8-711-BAA-A

48-PIN QFN (7x7)









(UNIT:mm)

ITEM	DIMENSIONS
D	7.00
E	7.00
A	0.90 MAX.
A1	0.05 MAX.
b	$0.25^{+0.05}_{-0.07}$
c	0.20
e	0.50
f	0.10
Lp	0.40±0.05
x1	0.10
x2	0.05
y	0.08
D2	5.70
E2	5.70

5. RECOMMENDED SOLDERING CONDITIONS

The μPD720201 and μPD720202 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact a Renesas Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.renesas.com/prod/package/manual/)

- μPD720201K8-701-BAC-A : 68-PIN QFN (8x8)
- μPD720202K8-701-BAA-A : 48-PIN QFN (7x7)
- μPD720201K8-711-BAC-A : 68-PIN QFN (8x8)
- μPD720202K8-711-BAA-A : 48-PIN QFN (7x7)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Peak package's surface temperature: 260°C, Reflow time: 60 seconds or less (220°C or higher), Maximum allowable number of reflow processes: 3, Exposure limit **Note**: 7 days (10 hours pre-backing is required at 125°C afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR60-107-3

Note The Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

REVISION HISTORY	μPD720201/μPD720202 Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	Dec. 7, 2010	-	First Edition issued
0.02	Apr. 21, 2011	-	● Chapter1 ➢ Updated ordering information. ● Chapter2 ➢ Updated Table 5-1. SPI Interface ● Chapter4 ➢ Updated Package information.
0.03	June 6, 2011	-	● Chapter 1 ➢ Changed the revision of USB Battery Charging Specification ● Chapter 5 ➢ Updated the Recommended Soldering Condition Information
0.04	September 16, 2011	-	● Chapter 1 ➢ Updated the section 1.2 Applications ● Chapter 2 ➢ Modified the misdescription of SMIB (I/O Type) of Table 2-4. System Interface Signal. ● Chapter 3 ➢ Updated the SPI Type Serial ROM Interface ➢ Updated the Power Consumption
1.00	September 26, 2011	-	● Document promoted from Preliminary Data to full Data. (Document No. R19DS0047E) ● Chapter 3 ➢ Modified the misdescription OCIxB of the section 3.1 Buffer List
2.00	March 2, 2012	-	● Chapter 1 ➢ Modified the typo of part number of section 1.5 Pin Configuration ● Chapter 2 ➢ Changed the Function of SPISO of Table 2-7. SPI Interface

<table>
<tr><th rowspan="2">Rev.</th><th rowspan="2">Date</th><th colspan="2">Description</th></tr>
<tr><th>Page</th><th>Summary</th></tr>
<tr><td>3.00</td><td>May 25, 2012</td><td>-</td><td>● Chapter 1
➢ Updated 1.3 Ordering Information
➢ Updated 1.5 Pin Configuration (TOP VIEW)
● Chapter 3
➢ Updated the Operating Temperature Table 3-5. Recommended Operating Ranges
➢ Deleted the condition of Table 3-6. DC Characteristics
➢ Deleted the condition of Table 3-9. System clock (XT1/XT2) ratings
➢ Deleted the condition of Table 3-11. Power on Reset (PONRSTB) Timings
➢ Change the parameter name & value of Table 3-13. PCI Express Interface -Power-Up and PECREQB Signal Timings
➢ Added the remark to Figure 3-9. Power Up and Reset
● Chapter 4
➢ Added the part number
● Chapter 5
➢ Added the part number</td></tr>
<tr><td>4.00</td><td>September 20, 2012</td><td>-</td><td>● Chapter 3
➢ Deleted the description of section 3.9</td></tr>
<tr><td>5.00</td><td>January 17, 2013</td><td></td><td>● Chapter 1
➢ Updated 1.1 Features
➢ Added “Note” to 1.3 Ordering Information
● Chapter 3
➢ Updated Table3-25 SPI Type Serial ROM Interface Signals Timing (SPI Mode 0)
➢ Added Figure 3-21 SPISO Pull-up Timing from SPICSB disabled
● All Chapters
➢ Modified the typo</td></tr>
<tr><td>6.00</td><td>January 29, 2014</td><td>-</td><td>● Chapter 3
➢ Added the section 3.8.11 Overcurrent</td></tr>
</table>

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